UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,039	11/14/2001	Craig Nemecek	CYPR-CD01222M	1791

7590 06/06/2005	EXAMINER
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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
	10/004,039	NEMECEK ET AL.
Office Action Summary	Examiner	Art Unit
	Jason Proctor	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL.**   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-19_ is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-19_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _14 November 2001_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a) ☐ All   b) ☐ Some * c) ☐ None of:

       1. ☐ Certified copies of the priority documents have been received.

       2. ☐ Certified copies of the priority documents have been received in Application No. _____.

       3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 have been presented. Claims 1-19 have been rejected.

Oath/Declaration

1.   The oath or declaration is defective. A new oath or declaration in compliance

with 37 CFR 1.67(a) identifying this application by application number and filing date is

required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The date of signature for inventor Craig Nemecek is illegible.

The signature for inventor Steve Roe is missing.

Priority

2.   This Application contains a claim for the benefit of priority to U.S. Provisional

Application No. 60/243,708 filed 26 October 2000. The provisional application has been

reviewed and priority is denied, because the provisional application does not appear to

enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph.

See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style'

drawings and datasheets describing desired features for a microcontroller or a 'system-

on-chip,' but this material does not appear to contain either the text description or the

drawings found in the Application. In particular, no part of the provisional application

appears to disclose the method steps shown in the Application at Fig. 7.

Claim Objections

3.   Applicant is advised that should claim 3 be found allowable, claim 7 will be

objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two

claims in an application are duplicates or else are so close in content that they both

cover the same thing, despite a slight difference in wording, it is proper after allowing

one claim to object to the other as being a substantial duplicate of the allowed claim.

See MPEP § 706.03(k). Claim 7 explicitly recites the limitations of claims 2 and 3,

however claim 3 depends from claim 2. 37 CFR 1.75 states, "Claims in dependent form

shall be construed to include all the limitations of the claim incorporated by reference

into the dependent claim", therefore the limitations of claim 3 and 7 are identical.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

4.   Claims 3, 7-10, and 15-19 are rejected under 35 U.S.C. § 112, first paragraph, as

failing to comply with the written description requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application

was filed, had possession of the claimed invention. Claims 3, 7, and 15 recite a

limitation including the phrase "replacing the microcontroller clock with the gatekeeper

clock for clocking the virtual microcontroller when a watchdog event occurs" which is inadequately described by the disclosure. The claim seems to imply that the microcontroller clock drives the virtual microcontroller, a connection which is neither recited by these claims nor, in the case of claims 3 and 7, by any claim from which they depend.

Claims 8-10 stand rejected by virtue of their dependence upon claim 7.

Claims 16-19 stand rejected by virtue of their dependence upon claim 15.

5.   Claims 3, 7-10, and 15-19 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 3, 7, and 15 recite a limitation related to gatekeeper circuit switching means for replacing a clock on a microcontroller with a clock from another device. This limitation appears to be directed to physically replacing a tangible component of a tangible microcontroller with a second tangible component from a second tangible device. A person of ordinary skill in the art of software debugging would be unable to make and use an in-circuit emulation system that involves a gatekeeper circuit that physically replaces the components of microcontrollers or other electronic devices.

Claims 8-10 stand rejected by virtue of their dependence upon claim 7.

Claims 16-19 stand rejected by virtue of their dependence upon claim 15.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

6.   Claims 3, 7-10, and 15-19 are rejected under 35 U.S.C. § 112, second
paragraph, as being indefinite for failing to particularly point out and distinctly claim the
subject matter which applicant regards as the invention. Claims 3, 7, and 15 recite a
limitation including the phrase "switching means for replacing the microcontroller clock
with the gatekeeper clock for clocking the virtual microcontroller when a watchdog event
occurs" which at least vague and indefinite. This limitation appears to imply that the
microcontroller clock actually drives the virtual microcontroller, however there is no clear
recitation of that structure. It is not clear what is meant by replacing a microcontroller
clock with the gatekeeper clock. A clock is known in the art as a tangible device which,
in the context of microprocessors, generates a periodic pulse signal. A clock is typically
incorporated into the design of a computer system and nothing in the disclosure or the
claims suggests that Applicants' invention actually replaces on clock with another clock.
It is entirely unclear which clocks are driving what devices as recited by claims 3, 7, and
15. Clarification is respectfully requested.

Claims 8-10 stand rejected by virtue of their dependence upon claim 7.

Claims 16-19 stand rejected by virtue of their dependence upon claim 15.

7.   Claims 5-6, 9-10, 12-13, and 17-18 are rejected under 35 U.S.C. § 112, second
paragraph, as being indefinite for failing to particularly point out and distinctly claim the
subject matter which applicant regards as the invention.

The following regards claim 5 as exemplary of claims 9, 12, and 17, while claim 6 is regarded as exemplary of claims 10, 13, and 18.

Claim 5 recites a limitation including "detecting that the microcontroller clock is not active" which implies a relative measure that is not defined by the claim. A microcontroller clock, as known in the art, produces a periodic pulse signal. Even during what would be recognized as normal operation, the microcontroller clock is not active for the majority of the time between periodic pulses. The Examiner presumes this limitation refers to a microcontroller clock that is somehow not being used in normal operation, but the claim merely recites "not active". Further, it is known in the art to vary the clock rate for a number of reasons, such as to minimize power consumption. In doing so, the period between pulses increases and the microcontroller clock is "not active" for a greater length of time between pulses. The methods by which the gatekeeper determines that the microcontroller clock is "not active" are indefinite.

Further regarding claim 5, it is unclear how or why patentable weight should be granted to the limitation "and that a data bus is in a prescribed logic state". The claims do not recite any connection between previously recited elements or steps and the data bus of claim 5. It is unclear whether this is a data bus completely internal to the gatekeeper circuit or a data bus between, for example, the microcontroller and the host computer of claim 1.

Claim 6, depending from claim 5, recites further limitations pertaining to the data bus but does not clarify the indefiniteness of claim 5. The Examiner respectfully observes that the limitations of claim 6 regarding the data bus are clearly commensurate in scope with the teachings of the disclosure, however it is impossible to

make a similar analysis of the limitations of claim 5 because of the great deal of

indefiniteness. In resolving the issues for claim 5, the Examiner respectfully suggests

considering combining the limitations of claim 6 with claim 5 to ensure that the scope of

the claims is commensurate with the teachings of the disclosure.

8.   Claim 18 recites the limitation "the data bus" in line 1. There is insufficient

antecedent basis for this limitation in the claim. The Examiner presumes claim 18

should properly depend from claim 17 following the pattern of claims 5-6, 9-10, and 12-

13.

Claim Interpretation

In the interest of compact prosecution, the Examiner makes the following claim

interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*,

222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

9.   Regarding claims 3, 7, and 15, the Examiner cannot interpret this claim without

relying on speculative assumptions and therefore cannot productively apply prior art to

this claim. See *In re Steele*, 305 F.2d 859,134 USPQ 292 (CCPA 1962).

10.   Regarding claims 8-10 which depend from claim 7, the Examiner cannot interpret

these claims without relying on speculative assumptions for claim 7. However, in the

interests of compact prosecution, the Examiner has presented prior art that teaches the

specific limitations recited by claims 8-10.

11.   Regarding independent claim 15, the Examiner has interpreted the limitation of "disabling a microcontroller clock signal" as "halting the microcontroller and running the virtual microcontroller" in the interests of compact prosecution.

12.   Regarding claims 5, 9, 12, and 17 the limitations are so different from the teachings of the disclosure that the Examiner cannot interpret them except in the most general terms to avoid reading the specification into the claims.   Therefore the limitations of these claims are interpreted as "wherein the gatekeeper circuit detects that a watchdog event has occurred by monitoring the state of the microcontroller".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13.   Claims 1-2, 4-6, and 8-19 rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,911,059 to Profit, Jr. (Profit).

14.   Regarding claim 1, Profit teaches an in-circuit emulation system including:

A microprocessor (column 6, lines 5-24, especially lines 18-19), the microprocessor has a clock count and therefore a clock (column 12, lines 24-35);

A virtual microprocessor (referred to as a *processor model shell 212*) (column 6, lines 25-32) running in lock-step with the microprocessor (column 11, lines 40-43);

A host computer running in-circuit emulation debug software (column 6, lines 25-60), the host computer being in communication with the virtual microcontroller (Fig. 7, reference 220; column 5, line 58 – column 6, line 4); and

A gatekeeper circuit (referred to as *RUN/HALT controller 240*) coupled to the virtual microcontroller and the microcontroller (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as *time keeper circuit 232*) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Official notice is taken that the term *microcontroller* refers to a single unit usually comprising central processing unit, memory, and I/O ports. As Profit teaches an emulator unit that contains at least these features (Fig. 7, reference 202), it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention that Profit's emulator is readily adaptable to accept microcontrollers, as would be desired by a person whose goal it is to develop and debug code for microcontrollers.

Regarding claim 2, Profit teaches a gatekeeper clock running independent of the microcontroller clock to clock operations carried out in the gatekeeper circuit (column 10, lines 38-41, *"In this embodiment, the simulation time keeper circuit 232 includes a counter"*; column 10, lines 44-45, *"The counter is driven by the clock signal on line 242"*).

Regarding claim 4, Profit teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Regarding claims 5 and 6, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding the limitations specific to claim 8, Profit teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Regarding the limitations specific to claims 9 and 10, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

15.   Regarding claim 11, Profit teaches an in-circuit emulation system with a gatekeeper circuit (referred to as *RUN/HALT controller 240*) (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as *time keeper circuit 232*) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Profit also teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Profit also teaches sending a signal to the virtual microcontroller to resume its operation, functionally equivalent to providing a clock signal (column 10, lines 4-23).

Profit does not explicitly recite "permitting the host computer to query memory locations and registers of the virtual microcontroller", however Profit does explicitly recite that the host computer contains software debugging tools (column 6, lines 49-60). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine Profit's explicit suggestion, in combination with his own knowledge of the particular art, to include the memory and register probing means that are both well known in the art and necessary to adequately debug software for the microcontroller.

Regarding claims 12 and 13, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding claim 14, Profit teaches a gatekeeper clock running independent of the microcontroller clock to clock operations carried out in the gatekeeper circuit (column 10, lines 38-41, *"In this embodiment, the simulation time keeper circuit 232 includes a* counter"; column 10, lines 44-45, *"The counter is driven by the clock signal on line 242"*).

16.   Regarding claim 15, Profit teaches an in-circuit emulation system with a gatekeeper circuit (referred to as *RUN/HALT controller 240*) (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as *time keeper circuit 232*) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Profit also teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and

modify the teachings of Profit to arrive at the claimed limitation of "determining that a watchdog timer event has occurred in a microcontroller".

Profit also teaches a virtual microprocessor (referred to as a *processor model shell 212*) (column 6, lines 25-32) running in lock-step with the microprocessor (column 11, lines 40-43);

Profit also teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Profit also teaches notifying a host computer running in-circuit emulation software that a watchdog timer event has occurred (column 11, lines 56-61).

Regarding claim 16, Profit does not explicitly recite "permitting the host computer to query memory locations and registers of the virtual microcontroller", however Profit does explicitly recite that the host computer contains software debugging tools (column 6, lines 49-60). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine Profit's explicit suggestion, in combination with his own knowledge of the particular art, to include the memory and register probing means that are both well known in the art and necessary to adequately debug software for the microcontroller.

Regarding claims 17 and 18, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring

the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring "the data address and status lines on the target bus 208 of the processor emulator 202" (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding claim 19, Profit teaches a gatekeeper clock running independent of the microcontroller clock to clock operations carried out in the gatekeeper circuit (column 10, lines 38-41, *"In this embodiment, the simulation time keeper circuit 232 includes a counter"*; column 10, lines 44-45, *"The counter is driven by the clock signal on line 242"*).

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.
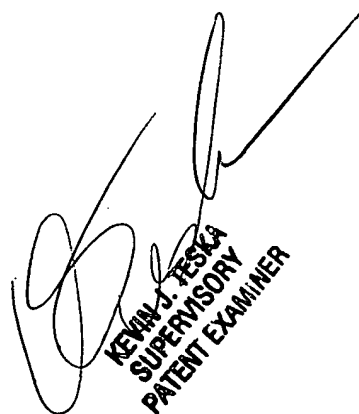
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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